ABSTRACT OF THE DISCLOSURE

A device and a method for processing high data rate serial data includes circuitry for recovering a clock based on the high data rate input data stream and for providing the recovered clock to a circuit portion, for example, a portion of a field programmable gate array fabric, to enable the circuit portion to use either a reference clock or the recovered clock for subsequent processing. The invention specifically allows for different circuitry portions to utilize different clocks, including different recovered clocks, for corresponding functions that are being performed. Applications for the present invention are many but include multi-gigabit transceiver, switching devices, and protocol translation devices. More generally, the device and method provide for application specific clock references to be utilized in order to minimize or eliminate timing mismatch in serial data processing.